

Homework 5

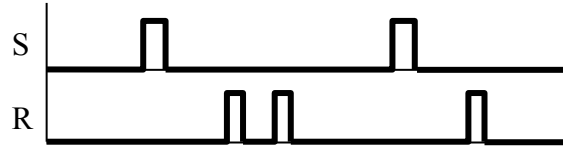
Assignment is due in class on Thursday, March 14, 2013

All questions in this homework require drawing, so it hardly makes sense to use CAPA...

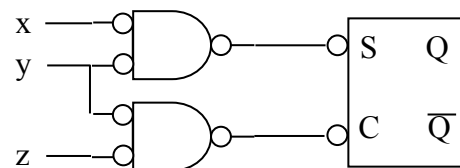
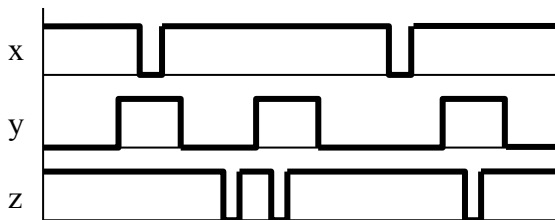
Make sure that what you hand in maintains the order of the problems given here.

Latches

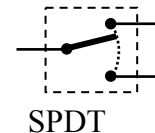
5-1 A NOR latch starts with $Q = 0$. Then, the inputs Set and Reset are varied as seen in this timing diagram. Redraw this diagram, with the output Q underneath it.



5-2 The waveforms below are applied to the circuit below. Assuming that $Q = 1$ initially, draw a timing diagram with both inputs and both outputs of the latch; your diagram will have 7 waveforms.

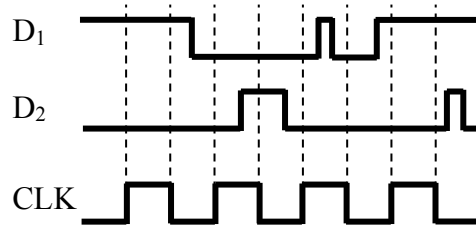


5-3 You want to de-bounce a SPDT switch using a NOR latch. You of course may also use resistors, ground, and V_{cc} . Draw the necessary circuit. Be very careful that your circuit never applies the “not permitted” input combination.

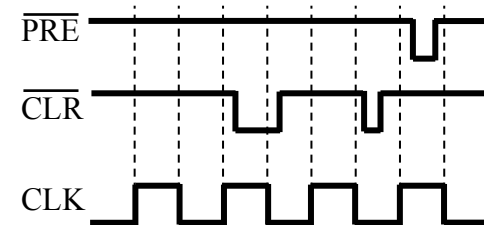


Flip-Flops

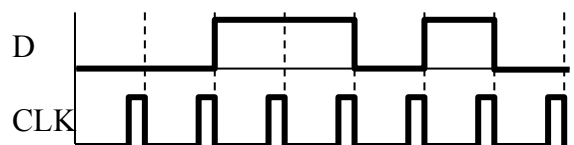
5-4 Copy the timing diagram to the right.
 a) Suppose the inputs D_1 and CLK are applied to a D flip-flop that triggers on positive-going transitions. At the bottom of the diagram show the Q output of the flip-flop, taking $Q_1=1$ initially.
 b) Repeat, with the inputs D_2 and CLK. Just add a single new trace to the diagram, labeled Q_2 .



5-5 Copy the timing diagram to the right, and below it show the Q output of a JK flip-flop that triggers on negative-going transitions, has its J and K inputs wired high, and has its other inputs as shown. Assume that $Q = 0$ initially.

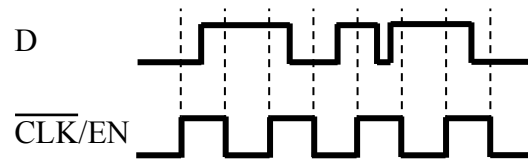


5-6 The following signals are applied to a D flip-flop with a negative transition trigger. Copy the timing diagram, and add to it the output Q , assuming that Q is initially low and that the flip-flop’s hold time is $t_H = 0s$. Then, draw a circuit that will delay the output by two clock periods.

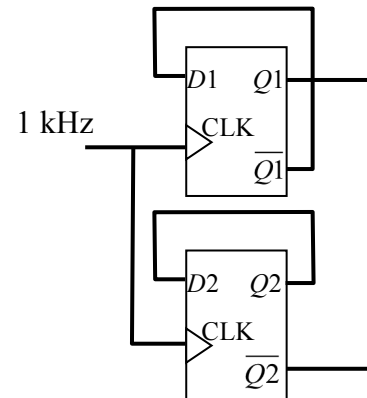


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- 5-7 Compare the operation of the D latch with a falling-edge-triggered D flip-flop by applying the waveforms to the right to each and determining the Q waveforms. Take the Q's to be initially low. Copy the timing diagram, and add your two (clearly labeled) outputs to it.



- 5-8 Two D flip-flops are connected as shown to the right. $Q1$ and $Q2$ are both initially low. Draw a timing diagram with CLK and the circuit outputs ($Q1$ and $\overline{Q2}$). Also, determine the frequency of those outputs. Assume that these flip-flops have a hold time of 0ns.



- 5-9 In the previous problem, you saw how to make a D-FF operate in a toggle mode. Explain why the same idea could not be implemented with a D latch.