Homework #3

Digital Electronics — Dr. Pogo

Assignment is due on Thursday, February 14, 2008 — Assigned February 7, 2008

Reading Assignment: Chapters 4-6 through 4-8, and 9-6 through 9-7 of *Digital Systems: Principles and Applications*, 10th edition, by Tocci, Widmer & Moss.

3-1 A circuit is desired for $Q = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}BC + A\overline{B}\,\overline{C} + A\overline{B}C$. Use a 74151 multiplexer to generate Q. Draw a picture indicating how you would connect each of the 16 pins on the 74151, similar to the example problem distributed in class. Switch "A" must be attached to MUX input "A",etc.

3-2 Use the 74153 Mux to create: $Q = \overline{X}YZ + WX\overline{Z} + W\overline{X}Y\overline{Z} + X\overline{Y} + \overline{W}\,\overline{Y}Z$
The inputs of your truth table MUST be ordered WXYZ, reading left to right. You may use both MUXes on the 74153, two inverters, and one OR gate.

3-3 Solve problems 3-1 and 3-2 in *Digital Works*, in one file. As usual, save it as **abc23-assign03.dwm**, where **abc23** is your Geneseo email name, in my inbox. Also, make sure that your name is in a text box in the circuit itself.

3-4 The 74151 chip is a "1of 8" MUX: there are 8 inputs, and 1 output. We want to build a circuit that acts as a 1 of 64 MUX. This MUX has to be generic, so that it can be used to solve a*ny* truth table. Therefore, we can't use our usual MUX tricks to increase the capabilities of the 74151 MUX.
Design a group of chips that as a group, has 6 Select inputs, 64 Data Inputs, and 1 output. To build this group, you may use several 74151 chips, and no other gates. You must *explicitly* show how every Data and Select input is connected. Look up "explicit" in the dictionary if you don't know what it means.

3-5 Use Karnaugh maps to generate expressions for Q for these two truth tables. An "X" indicates "don't care", so your solution is permitted to generate either a 0 or a 1 there, depending on which results in a simpler expression.

A	B	C	R
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	X
1	1	0	1
1	1	1	0

A	B	C	D	R
0	0	0	0	1
0	0	0	1	1
0	0	1	0	X
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

3-6 Design a *3-bit magnitude comparator*. It has 6 inputs and 3 outputs. In other words, write Boolean expressions for the 3 outputs M, N, and P. You may use XORs and/or XNORs. The required inputs and outputs are:
- <u>inputs</u>: $x_2\, x_1\, x_0$: the bits of a single 3 bit number;
- <u>inputs</u>: $y_2\, y_1\, y_0$: the bits of another single 3 bit number;
- <u>output</u>: M: true if $x_2x_1x_0 = y_2y_1y_0$;
- <u>output</u>: N: true if $x_2x_1x_0 > y_2y_1y_0$;
- <u>output</u>: P: true if $x_2x_1x_0 < y_2y_1y_0$.

The subscript zero indicates the LSB of any number.

Example: if $x_2x_1x_0 = 101\ (5_{10})$ and $y_2y_1y_0 = 110\ (6_{10})$, then M = N = 0, P =1.
Example: if $x_2x_1x_0 = 011\ (3_{10})$ and $y_2y_1y_0 = 000\ (0_{10})$, then M = P = 0, N =1.

3-7 Design a *2-bit multiplier*. It has 4 inputs and 4 outputs. In other words, write Boolean expressions for the 4 outputs $z_3\, z_2\, z_1\, z_0$. The inputs and outputs are:
- <u>inputs</u>: $x_1\, x_0$: the bits of a single 2 bit number;
- <u>inputs</u>: $y_1\, y_0$: the bits of another single 2 bit number;
- <u>output</u>: $z_3\, z_2\, z_1 z_0$: the bits of a 4 bit number.

Example: if $x_1\, x_0 = 10\ (2_{10})$ and $y_1\, y_0 = 11\ (3_{10})$, then $z_3\, z_2\, z_1 z_0 = 0110\ (6_{10})$.
Example: if $x_1\, x_0 = 01\ (1_{10})$ and $y_1\, y_0 = 10\ (2_{10})$, then $z_3\, z_2\, z_1 z_0 = 0010\ (2_{10})$.