Homework #4

Digital Electronics — Dr. Pogo

Assignment is due on Tuesday, March 26, 2008 — Assigned February 14, 2008

Reading Assignment: Chapters 9-1 through 9-2, and 5-1 through 5-5 of *Digital Systems: Principles and Applications*, 10th edition, by Tocci, Widmer & Moss.

Decoders:

4-1 Consider a 74138 decoder chip with select inputs $A_2A_1A_0$ and enable inputs $\overline{E_2}\ \overline{E_1}\ E_0$. Determine the state of all 8 outputs when:

a. all six inputs are low;

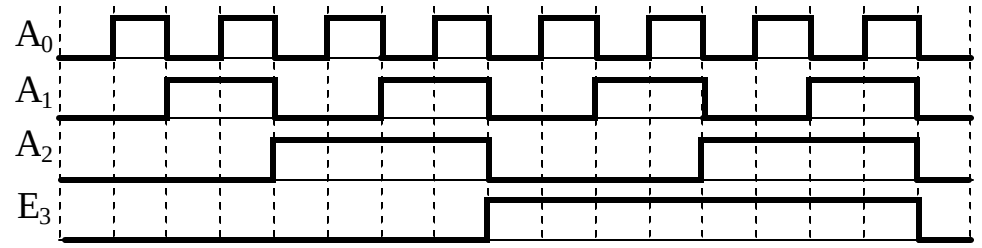
b. Five inputs are low, but E_3 is high.

c. Four inputs are high, but $\overline{E_2}$ = $\overline{E_1}$ = low

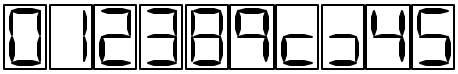
d. All six inputs are high.

4-2 Using only 74138 chips, wires, ground, and Vcc, design a 1-of-16 decoder. There should be four select inputs $D_2D_2D_1D_0$ and one (active low) enable input E_1.

4-3 A 74138 decoder has $\overline{E_2}$ = $\overline{E_1}$ = low. The other four inputs vary as seen in this timing diagram. Redraw these timing diagrams, and lined up below them, draw the outputs $\overline{O_0}$, $\overline{O_3}$, $\overline{O_6}$, and $\overline{O_7}$.



4-4 You attempt to wire a 7447 BCD driver to a 7-segment display device. While you expect to see regular numbers from 0 to 9, you instead see the following. Determine what mistake was made during the wiring process.

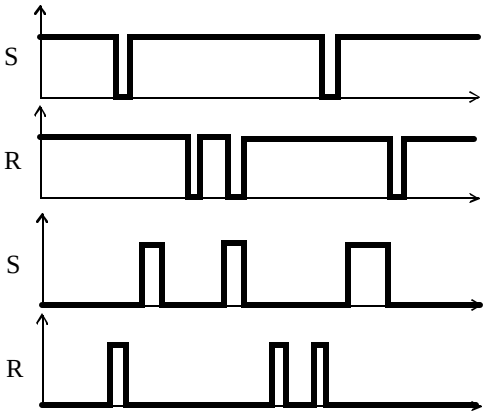


4-5 Repeat problem 4-4 for this output:

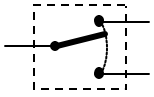
Latches:

4-6 A NAND latch starts with Q = 0. Then, the inputs Set and Reset are varied as seen in this timing diagram. Redraw this diagram, with the output Q underneath it.

4-7 A NOR latch starts with Q = 0. Then, the inputs Set and Reset are varied as seen in this timing diagram. Redraw this diagram, with the output Q underneath it.



4-8 You want to debounce a SPDT switch using a NOR latch. You of course may also use resistors, ground, and Vcc. Draw the necessary circuit.



SPDT Switch