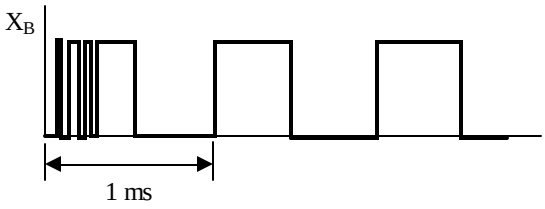
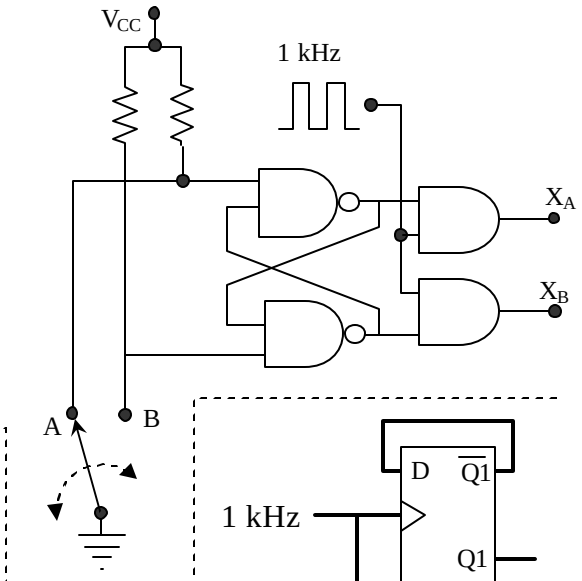
Homework #5

Digital Electronics — Dr. Pogo

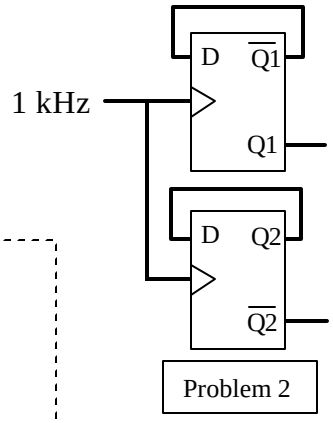
Assignment is due on Thursday, April 3, 2008 — Assigned March 6, 2008

1. The circuit shown is a switching circuit, but it is not functioning as designed. When the switch is moved from A to B, X_B appears as follows. What is the probable hardware error that would cause this behavior?



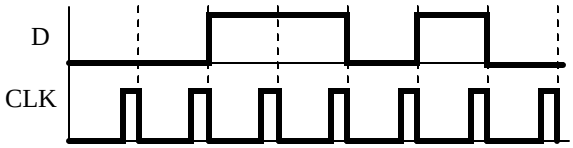


2. Two D Flip-Flops are connected as shown. The outputs of both Flip-Flops (Q1, Q2) are initially low. Under a timing diagram of CLK, draw the waveform of Q1 and Q2. Also, determine the frequency of Q1 and Q2.

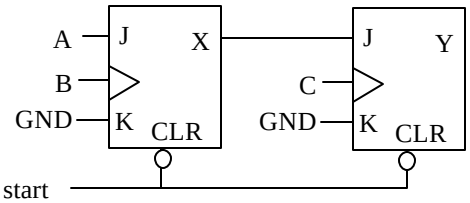


Problem 2

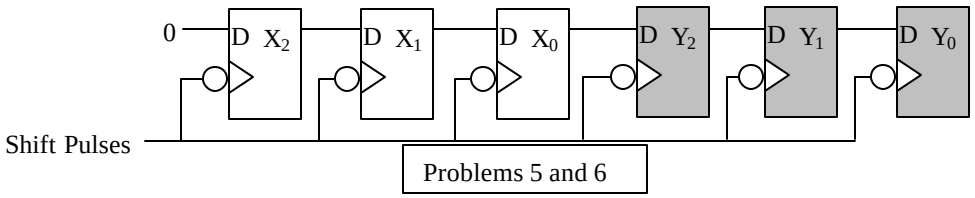
3. The following signals are applied to a D flip-flop. Draw the output Q. Then, draw a circuit that will delay the output by two clock periods.



4. The two JK flip-flops form a combination lock; the output Y will go high only when the inputs A, B, and C are changed to high in a particular sequence. The inputs A, B, and C into the two JK flip-flops all start low. Determine the correct sequence. Also, explain the function of the "start" input. Finally, design a circuit with the same function using D flip flops instead of JK flip flops.



5. Three bits of data are stored in X_2-X_1-X_0. After 3 shift pulses, this data is moved onto Y_2-Y_1-Y_0, and X_2-X_1-X_0 are replaced with 000. Modify this circuit so that the original data ends up in both the X and Y registers instead of only the Y register.



Problems 5 and 6

6. Suppose that $X_2X_1X_0Y_2Y_1Y_0$ is initially 100011. After four shift pulses, it becomes 001111. After that, subsequent shift pulses produce no change. This is not the expected result. What is the probable fault in this circuit?

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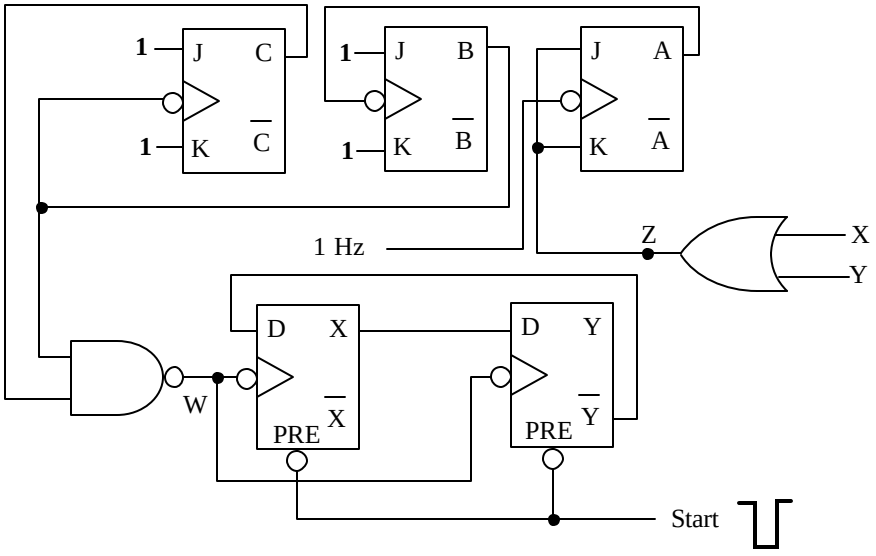
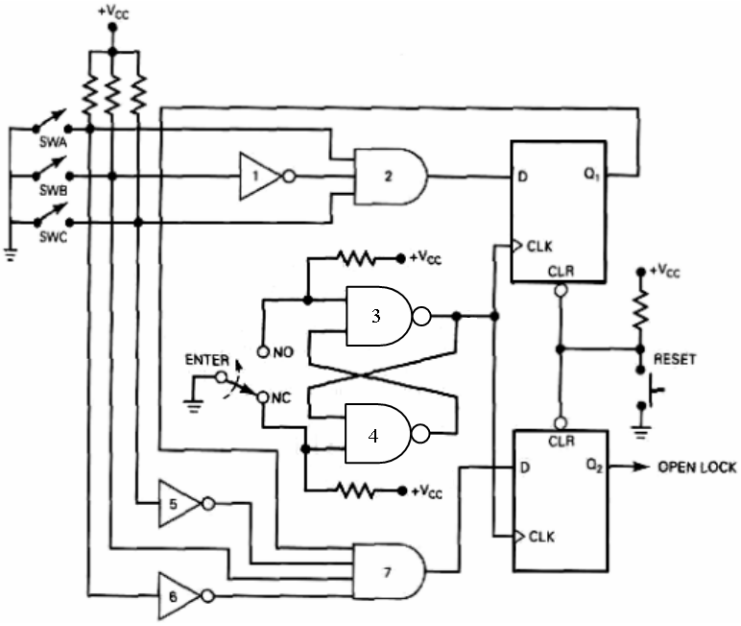
7. All of the flip-flops are initialized to zero. Then, the start pulse is triggered. Make timing diagrams/plots of A, B, C, X, Y, W, and Z for 20 cycles after the start pulse.



8. A 555 oscillator can be used to generate an oscillating signal, but it will not have a 50% duty cycle. Design a circuit using both a 555 and a JK flip flop to produce a square wave of 40 kHz frequency and 50% duty cycle. Show the values of any resistors or capacitors you choose, and explain why you chose them.

9. Here is another combination lock. The operation is: press reset (momentary), then set switches A, B, and C to combination 1, then toggle the enter switch, then set A, B, C to combination 2, then toggle the enter key again. Determine the necessary combinations 1 and 2. What happens if incorrect combinations are entered? Finally, build a similar circuit in **digitalworks** having combinations 011, 110.



10. You think you build this circuit correctly, but after testing, you discover it does not work. In particular, you discover that after entering the correct combination 1, Q_1 is high, but then entering the correct combination 2 results in only a momentary pulse at Q_2. What is the probable cause of this problem?